Confined Spacers for Double Gate Transistor Semiconductor Fabrication Process

ABSTRACT

A semiconductor fabrication process includes forming a silicon fin overlying a substrate. A gate dielectric is formed on primary faces of the fin. A gate electrode is formed over at least two faces of the fin. Dielectric spacers are then selectively formed in close proximity and confined to the sidewalls of the gate electrode thereby leaving a majority of the primary fin faces exposed. Thereafter a silicide is formed on the primary fin faces. The forming of the gate electrode in one embodiment includes depositing polysilicon over the fin and substrate, depositing a capping layer over the polysilicon, patterning photoresist over the capping layer and etching through the capping layer and the polysilicon with the patterned photoresist in place wherein the etching produces a polysilicon width that is less than a width of the capping layer to create voids under the capping layer adjacent sidewalls of the polysilicon where the confined spacers can be formed.